PATENTS
ALT-275

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION

Applicants : Steven Wilton et al.

Application No. : 10/649,401 Confirmation No. : 6103

Filed : August 26, 2003

For : METHOD FOR CONSTRUCTING AN INTEGRATED CIRCUIT DEVICE HAVING FIXED AND PROGRAMMABLE LOGIC PORTIONS AND PROGRAMMABLE LOGIC ARCHITECTURE FOR USE THEREWITH

Group Art Unit : 2819

New York, New York 10020
March 24, 2004

Hon. Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, applicants hereby make the following publications of record in the above-identified patent application:

Wilton, S.J.E., et al., "Programmable Logic IP Cores in SoC Design: Opportunities and Challenges", Proceedings of the IEEE 2001 Custom Integrated Circuits Conference, pp. 63-66 (May 2001)

Phillips, S., et al., "Automatic Layout of Domain-Specific Reconfigurable Subsystems for System-on-a-Chip", Tenth ACM International Symposium on Field-Programmable Gate Arrays, pp. 165-173 (February 2002)

Ghodrat, M., et al., "The Automatic FPGA Generator", Proceedings of the 5th Annual International Computer Society of Iran Computer Conference, pp. 3-10 (2000)

Copies of the aforementioned publications (including an English translation of the Ghodrat et al. article), which are listed on the accompanying Form PTO-1449 (submitted in duplicate), are enclosed herewith.

It is respectfully requested that these publications be (1) fully considered by the Patent and Trademark Office during examination of this application; and (2) printed on any patent which may issue on this application. Applicants request that a copy of Form PTO-1449, as considered and initialled by the Examiner, be returned with the next communication.

An early and favorable action is respectfully requested.

Respectfully submitted,

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I hereby certify that this Correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope Addressed to: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 on March 24, 2004

Claire J. Santil-van Goodman

Signature of Person Signing

FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. ALT-275	APPLN. NO. 10/649,401
INFORMATION DISCLOSURE STATEMENT BY APPLICANTS	APPLICANTS Steven Wilton et al.	CONF. NO. 6103
	FILING DATE August 26, 2003	GROUP ART UNIT 2819

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL	
	Wilton, S.J.E., et al., "Programmable Logic IP Cores in SoC Design: Opportunities and Challenges", Proceedings of the IEEE 2001 Custom Integrated Circuits Conference, pp. 63-66 (May 2001)
	Phillips, S., et al., "Automatic Layout of Domain-Specific Reconfigurable Subsystems for System-on-a-Chip", Tenth ACM International Symposium on Field-Programmable Gate Arrays, pp. 165-173 (February 2002)
	Ghodrat, M., et al., "The Automatic FPGA Generator", Proceedings of the 5th Annual International Computer Society of Iran Computer Conference, pp. 3-10 (2000)

EXAMINER DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicants.